

INFORMATION DISCLOSURE CITATION IN AN APPLICATION (PTO-1449)			ATTY. DOCKET NO. 57454-962		SERIAL NO. Divisional of Appln. Serial No. 09/986,865 10/622473	
			APPLICANT Hideto HIDAKA			
			FILING DATE July 21, 2003		GROUP 2824 Not yet assigned	

U.S. PATENT DOCUMENTS						
EXAMINER'S INITIALS	PATENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE
VTN	6,046,929	04/2000	Aoki et al.			
VTN	6,349,054	02/2002	Hidaka			

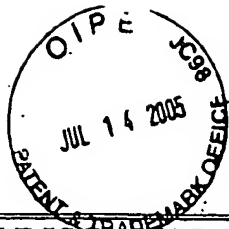
FOREIGN PATENT DOCUMENTS							
EXAMINER'S INITIALS	PATENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
						Yes	No

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)	
VTN	Scheuerlein, et al. "A 10ns Read and Write Non-Volatile Memory Array Using A Magnetic Tunnel Junction and FET Switch in Each Cell," ISSCC Digest of Technical Papers, TA7.2, February 2000, pages 94-95, 128-129 and 409-410
VTN	Durlam, et al., "Nonvolatile RAM Based on Magnetic Tunnel Junction Elements ISSCC Digest of Technical Papers, TA7.3, February 2000, pages 96-97, 130-131 and 410-411
VTN	Naji, et al, "A 256kb 3.0V iTiMTJ Nonvolatile Magnetoresistive RAM," ISSCC Digest of Technical Papers, TA7.6, February 2001, pages 122-123 and 438
	Co-Pending US Patent Application Serial Number 09/887,321, Filed June 25, 2001 see PTO

EXAMINER 	DATE CONSIDERED 9/15/05
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EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.



SHEET 1 OF 1

INFORMATION DISCLOSURE
"CITATION IN AN
APPLICATION

(PTO-1449)

ATTY. DOCKET NO.
057454-0962SERIAL NO.
10/622,473APPLICANT
Hideto HIDAKAFILING DATE
July 21, 2003GROUP
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EXAMINER'S INITIALS	CITE NO.	Document Number Number-Kind Codes (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
VTN		US 6,188,615 B1	02/13/2001	Perner et al.	
		US 6,128,239	10/03/2000	Perner	
		US 6,185,143	02/6/2001	Perner et al.	
		US 5,173,873	12/22/1992	Wu et al.	
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VTN		US 6,349,054 B1	02/19/2002	Hidaka	Corresponds to DE 101 30 829 A1

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EXAMINER'S INITIALS	CITE NO.	Foreign Patent Document Country Codes-Number -Kind Codes (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines Where Relevant Figures Appear	Translation	
						Yes	No
VTN		EP 1 104 092 A2	05/30/2001	HEWLETT-PACKARD COMPANY, A DELAWARE CORPORATION		X	
VTN		DE 199 14 488 C1	05/31/2000	SIEMENS AG	Corresponds to USP 2002/0093848 A1		X
VTN		DE 101 30 829 A1	07/18/2002	MITSUBISHI DENKI K.K.	Corresponds to 6,349,054 B1		X

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER'S INITIALS	CITE NO.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.
VTN		Durlam, M. et al., "Nonvolatile RAM based on magnetic tunnel junction elements" IEEE International Solid-State Circuits Conference, 7 to 9 February 2000, pp. 128-129.
VTN		Scheuerlein, R. et al., "A 10ns read and write nonvolatile memory array using a magnetic tunnel junction and FET-switch in each cell" IEEE International Solid-State Circuits Conference, 7 to 9 February 2000, pp. 128-129.
VTN		Yamada, K. et al., "A novel sensing scheme for a MRAM with a 5% MR ratio" Symposium on VLSI Circuits, 14 to 16 June 2001, pp. 123-124.
VTN		Zhang, R. et al., "Windowed MRAM sensing scheme" IEEE International Workshop on Memory and Technology, Design and Testing, 7 to 8 August 2000, pp. 47-55.
VTN		Kawashima, S. et al., "A charge-transfer amplifier and an encoded-bus architecture for low-power SRAM's" IEEE Journal of Solid-State Circuits, Vol. 33, No. 5, May 1998, pp. 793-799.

EXAMINER

DATE CONSIDERED

9/15/05

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1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.